WHAT IS CLAIMED IS:

1. A circuit, comprising:

an output node having an output voltage;

a set of transistors operative to control the signal level on the output node;

a quiet voltage supply providing a quiet voltage;

a noisy voltage supply providing a noisy voltage;

a pre-driver voltage supply, wherein the pre-driver voltage supply has a higher voltage than either the quiet voltage supply or the noisy voltage supply; and

a hot socket detect circuit to identify when the quiet, noisy or pre-driver voltage supply is below a predetermined value indicative of a hot socket condition and in response thereto generating control signals that place the set of transistors in a high impedance state in response to the hot socket condition.

2. The circuit of claim 1 wherein the set of transistors comprise:

a pull-up transistor connected to the output node; and

a pull-down transistor connected to the output node.

3. The circuit of claim 2 wherein a first pre-driver is connected to the pull-up transistor and a second pre-driver is connected to the pull-down transistor, wherein the first and second pre-drivers control the voltage supplied to the pull-up and pull-down transistors; wherein

the pre-driver voltage supply provides a pre-driver voltage to the first and second pre-drivers.

4. The circuit of claim 3 wherein the hot socket detection circuit passes the control signals to the first and second pre-drivers, and in response thereto, the first and second pre-drivers turn off the pull-up and pull-down transistors to establish the high impedance state.

5. The circuit of claim 4 wherein the hot socket detection circuit comprises:

a control signal node;

at least four input nodes, the input nodes including a pin node having as input the output voltage, a VCCQ node having as input the quiet voltage, a VCCN node having as input the noisy voltage and a VCCPD node having as input the pre-driver voltage;

a well bias circuit having the pin, VCCN and VCCPD nodes as input nodes and a VWELL voltage at a VBIAS output node;

a first, second and third hot socket detect block having an output HOT1, HOT2 and HOT3 respectively, each hot socket detect block having two input signals P1 and P2.

6. The circuit of claim 5 wherein the hot socket detection circuit further comprises an NOR gate having the HOT1, HOT2 and HOT3 as inputs and an inverter connected to the NOR gate, the inverter having as input an output of the NOR gate and a control signal as an output.

7. The circuit of claim 6 wherein the NOR gate and the inverter are powered by VWELL.

8. The circuit of claim 5 wherein the well bias circuit comprises

a first group of transistors having inputs from the pin and the VCCN nodes, wherein the first group of transistors provide an output voltage BIAS1, BIAS1 being a higher voltage of voltages at the VCCN and pin nodes; and

a second group of transistors having as inputs the BIAS1 voltage and a voltage at the VCCPD node, wherein the second group of transistors provide the output voltage VWELL, VWELL being a higher voltage of the BIAS1 voltage and the voltage at the VCCPD node.

9. The circuit of claim 5 wherein the first hot socket detect block inputs P1 and P2 are the VWELL voltage and VCCPD node voltage, wherein the output HOT1 is

a digital low if P2 is a digital high; and

a digital high if P2 is a digital low.

10. The circuit of claim 5 wherein the second hot socket detect block inputs P1 and P2 are VCCN and VCCPD node voltages, respectively, wherein the output HOT2 is

a digital low if P2 is a digital high; and

a digital high if P2 is a digital low.

11. The circuit of claim 5 wherein the third hot socket detect block inputs P1 and P2 are the VCCPD and VCCQ node voltages, wherein the output HOT3 is

a digital low if P2 is a digital high; and

a digital high if P2 is a digital low.

12. A programmable logic device, comprising:
a plurality of logic array blocks;
interconnect circuitry linking the plurality of logic array blocks; and
a plurality of output buffers connected to the interconnect circuitry, at least one output buffer being the circuit of claim 1.

13. A printed circuit board on which is mounted a programmable logic device of claim 12.

14. The printed circuit board of claim 13 further comprising:
memory circuitry mounted on the printed circuit board and coupled to the programmable logic device.

15. The printed circuit board of claim 14 further comprising
Processing circuitry mounted on the printed circuit board and coupled to the memory circuitry.

16. A digital processing system comprising:
processing circuitry;
a memory coupled to the processing circuitry; and
a programmable logic device of claim 12 coupled to the processing circuitry and the memory.

17. An integrated circuit device comprising the buffer of claim 1.

18. A method of controlling integrated circuit output signal during a hot socket condition wherein the integrated circuit includes first, second and third input voltage signals, wherein the third input voltage signal is greater than either the first or the second input voltage signal, the circuit further having an output voltage at an output pad of the integrated circuit, the method comprising:

determining a VWELL voltage, the VWELL voltage being the highest of the output voltage, the first voltage, and the third voltage;

determining a HOT1 signal using the VWELL voltage and the third voltage;

determining a HOT2 signal using second and third voltages;

determining a HOT3 signal using the first and third voltages;

identifying a hot socket condition when either the HOT1 or HOT2 or HOT3 signal is a digital high signal.

19. The method of claim 18 wherein the first, second and third input voltages are a noisy voltage signal from a noisy voltage supply, a quiet voltage signal from a quiet voltage supply and a pre-driver voltage signal used to supply pre-drivers in a hot socket detect circuit, respectively.

20. A hot socket detect circuit, comprising:

a well bias circuit; and

a plurality of hot socket detect blocks

wherein the hot socket detect circuit indicates a hot socket condition if an output of any one of the plurality

of hot socket detect blocks provides a predetermined signal.